Claim 12 (Original) A semiconductor memory device according to claim 9, wherein a threshold voltage of said driver MOSFET is higher than a threshold voltage of said transfer MOSFET.

Claim 13 (Original) A semiconductor memory device according to claim 9, wherein an absolute value of the threshold voltages of said transfer MOSFET and said driver MOSFET is lower than an absolute value of a threshold voltage of said load MOSFET.

Claim 14 (Original) A semiconductor memory device according to claim 9, wherein a logic circuit including a first MOSFET having a first threshold voltage and a second MOSFET having a second threshold voltage higher than said first threshold voltage is packaged together on a substrate on which said memory circuit is disposed, and wherein said first MOSFET is used as said transfer MOSFET and said second MOSFET is used as said driver MOSFET.

Claim 15 (Currently Amended) A semiconductor memory device comprising a memory array in which static type memory cells comprised of a latch circuit including a pair of driver MOSFETs and a load device and two transfer MOSFETs accessing to the latch circuit ~~pair of driver MOSFET, a pair of transfer MOSFET and a pair of load devices~~ are arranged in an array-like manner, wherein the semiconductor memory device has a source potential control circuit for controlling a potential of a source line connected to a source electrode of said driver MOSFET;

TP wherein a MOSFET disposed in a first area in which said memory cells are arranged in a direction perpendicular to the bit line at one end of said memory array is provided, a portion of a gate layer of the MOSFET disposed in said first area is connected to a ground potential and the other portion of said gate layer is connected to a signal line for controlling an operational potential of the memory cells; and

wherein said source potential control circuit includes at least first and second elements connected in parallel to each other, said first element having a resistance less than a resistance of said second element and predetermined according to a value of Vth of said driver MOSFETs and said transfer MOSFETs.

Claim 16 (Original) A semiconductor memory device according to claim 15, wherein, in a layout pattern of said memory cells, said pair of driver MOSFETs, said pair of transfer MOSFETs and said pair of load devices are arranged symmetrically with respect to a predetermined point in the pattern of said memory cells.

Claim 17 (Previously Presented) A semiconductor memory device according to claim 15, wherein a portion of said MOSFET formed in said first area is used for the switch.